

**REMARKS**

Applicants thank the Examiner for examining the pending application. The Office Action dated April 27, 2009 has been received and its contents carefully reviewed.

**Summary of the Office Action**

Claims 1, 4, 5, 7-9 and 12-14 are pending, claim 1 is rejected, and claims 4, 5, 7-9 and 12-14 are withdrawn.

The Office Action rejects claim 1 under 35 U.S.C. 102(b) as anticipated by Hasegawa et al. (US 6,335,717 B1); or in the alternative, under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (US 6,335,717 B1) in view of Saishu et al. (US 5,949,391 A).

**Summary of the Response to the Office Action**

Applicants have amended claim 1 to further define the invention. No new matter has been added. Reconsideration of the pending claims is respectfully requested.

**Rejection Under 35 U.S.C 112, second paragraph**

The applicants have amended claim 1 to be clear to one having ordinary skill in the art.

**Rejection Under 35 U.S.C 102(b)/103(a)**

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "one data line is arranged between adjacent pixels, supplying a

plurality of gate voltages to the plurality of gate lines during an electric field alignment of the ferroelectric liquid crystal material, wherein each of the gate voltages is set at a level higher than a threshold voltage of the thin film transistor, the gate voltages are generated in a range of from ten to four-hundred times during the electric field alignment, and each gate voltage is simultaneously supplied to the plurality of gate lines; supplying a first data voltage for the electric field alignment to the plurality of data lines in response to each gate voltage, wherein a polarity of the first data voltage is inverted every time when the gate voltage is supplied; sequentially supplying a plurality of scan pulses to the plurality of gate lines during normal driving for image display, wherein each of the scan pulses is generated for one horizontal period and is supplied to one of the plurality of gate lines; and supplying a second data voltage for the image display to the plurality of data lines in response to each scan pulse, wherein a polarity of the second data voltage is inverted every time when the scan pulse is supplied”.

First, in the claimed invention, a plurality of gate voltages and a first data voltage are supplied during an electric field alignment, and then a plurality of scan pulses and a second data voltage are supplied during a normal driving. Hasegawa and Saishu, whether taken individually or in combination, fail to disclose at least this feature of the claimed invention.

Second, in the claimed invention, one data line is arranged between adjacent pixels. In Saishu, two signal lines 18 and 20 are arranged between adjacent pixels. Thus, Saishu fails to disclose at least this feature of the claimed invention.

Third, in the claimed invention, each gate voltage is simultaneously supplied to the plurality of gate lines. On the contrary, in Hasegawa, each signal  $V_g$  is supplied to two scanning lines 24 or scanning lines 24 contained in each group. In Saishu, each scan signal is supplied to one signal line. Thus, Hasegawa and Saishu, whether taken individually or in combination, fail to disclose at least each gate voltage simultaneously supplied to all of the gate lines of the claimed invention.

None of the cited reference, singly or in combination, discloses at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 1 is allowable over the cited references.

In the meantime, the non-final OA states that Applicants are requested in correcting any errors in the figures and the specification.

Applicants cannot regretfully find any errors in figures.

In addition, Applicants respectfully submit that definition of references Ion and Int off omitted in figure 14 is added to in the paragraph [0072] of the specification.

### **CONCLUSION**

In view of the foregoing, Applicants respectfully request reconsideration and the timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

**MORGAN, LEWIS & BOCKIUS LLP**

Dated: July 27, 2009

By: 

Xiaobin You  
Reg. No. 62,510

Customer No.: 009629  
**MORGAN, LEWIS & BOCKIUS LLP**  
1111 Pennsylvania Avenue, N.W.  
Washington, D.C. 20004  
Telephone: 202-739-3000  
Facsimile: 202-739-3001